On the Design and Performance of a 6–18 GHz Three-Tier Matrix Amplifier

KARL B. NICLAS, SENIOR MEMBER, IEEE, AND RAMON R. PEREIRA

Abstract—**A 3×3 matrix amplifier for the 6–18 GHz frequency band has been developed. Employing MESFET's fabricated on VPE material, gains of $G = 23.5 \pm 0.5$ dB with a maximum reflection loss of $RL = -10$ dB were obtained from 5.2 to 18.7 GHz. Gain improved to $G = 29.1 \pm 1.1$ dB at a worst-case reflection loss of $RL = -7.5$ dB between 4.6 and 18.3 GHz when MBE material was used for the MESFET's. In addition to the experimental results, important design considerations, especially in regard to the termination impedances of the idle ports, are discussed.**

I. Introduction

THE PRACTICALITY of a matrix amplifier with more than two tiers has been uppermost in our minds ever since the measurement of the first encouraging results achieved on the original two-tier matrix amplifiers [1]. Early theoretical studies predicted a somewhat reduced bandwidth capability of the three-tier matrix amplifier when compared with its two-tier equivalent. In spite of this, having fabricated and tested a good number of two-tier matrix amplifiers [2]–[4] and being reassured by their performance, we gathered enough momentum to focus our attention on the development of a 6–18 GHz three-tier module. The choice of the frequency band was influenced by such technical factors as the relatively easy task of achieving a very high gain performance using simple biasing circuitry and, of course, the band's widespread employment. Gain enhancement through the use of purely reactive terminations of selected idle ports and other measures responsible for the performance of the amplifier modules, as well as important experimental results, will be discussed in detail.

II. Principle of Operation

Deriving an accurate formula for the linear gain of the three-tier matrix amplifier in terms of its circuit and device parameters is a gigantic task that leads to extremely complicated results. Unfortunately, an interpretable expression requires significant concessions to accuracy and, consequently, depending on the parasitics of the active devices, renders qualitative answers at best. Starting with an accurate device model, we will strip the latter of most of its parasitics in order to arrive at a relatively simple formula for the gain. The results will then be used to qualitatively explain certain steps that were taken in the design of the 3×3 matrix amplifier module. Fig. 1 shows the schematic of an active eight-port that may be considered an elementary cell of the amplifier. Cascading several (n) of these cells and terminating all idle ports with the admittances Y results in the three-tier matrix amplifier of Fig. 2. Assuming identical gain cells, we obtain the termination voltages with the matrix equation

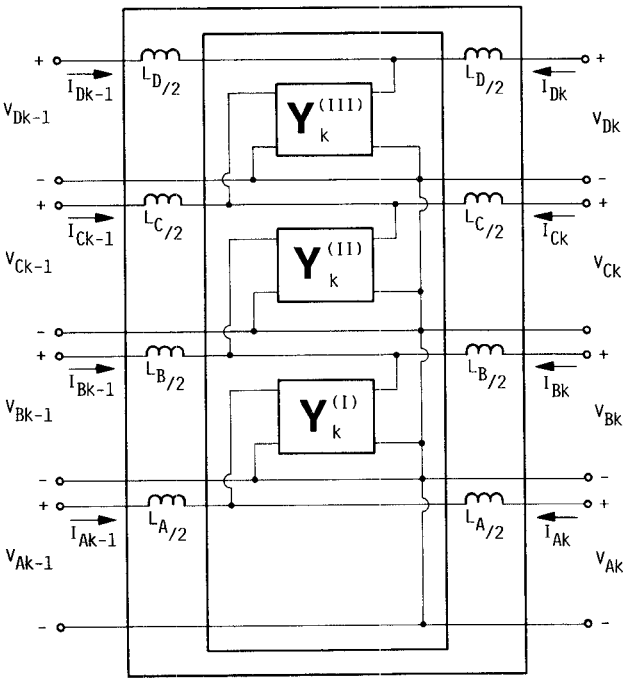

Fig. 1. Schematic of the elementary amplifier cell.

$$\begin{bmatrix} V_{D0} \\ -Y_{D0}V_{D0} \\ V_{C0} \\ -Y_{C0}V_{C0} \\ V_{B0} \\ -Y_{B0}V_{B0} \\ V_{A0} \\ I_{A0} \end{bmatrix} = A^n \begin{bmatrix} V_{Dn} \\ Y_L V_{Dn} \\ V_{Cn} \\ Y_{Cn}V_{Cn} \\ V_{Bn} \\ Y_{Bn}V_{Bn} \\ V_{An} \\ Y_{An}V_{An} \end{bmatrix} \tag{1a}$$

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The authors are with the Watkins-Johnson Company, Stanford Research Park, Palo Alto, CA 94304-1204.
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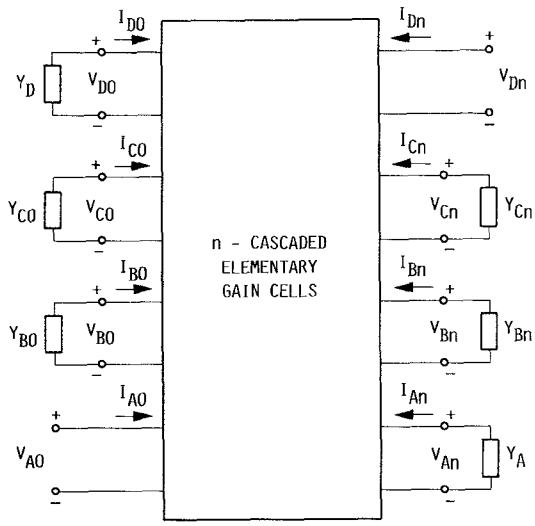


Fig. 2. The amplifier block and its terminations.

where

$$A = \left[\begin{array}{cc|cc} \left(1+j\frac{1}{2}\omega L_D Y_{22}\right) & j\frac{1}{2}\omega L_D\left(2+j\frac{1}{2}\omega L_D Y_{22}\right) & j\frac{1}{2}\omega L_D Y_{21} & -\frac{1}{4}\omega^2 L_D L_C Y_{21} \\ Y_{22} & \left(1+j\frac{1}{2}\omega L_D Y_{22}\right) & Y_{21} & j\omega\frac{1}{2}L_C Y_{21} \\ \hline j\frac{1}{2}\omega L_C Y_{12} & -\frac{1}{4}\omega^2 L_C L_B Y_{12} & \left[1+j\omega\frac{1}{2}L_C(Y_{11}+Y_{22})\right] & j\frac{1}{2}\omega L_C\left[2+j\omega\frac{1}{2}L_C(Y_{11}+Y_{22})\right] \\ Y_{12} & j\omega\frac{1}{2}L_D Y_{12} & (Y_{11}+Y_{22}) & \left[1+j\frac{1}{2}\omega L_C(Y_{11}+Y_{22})\right] \\ \hline 0 & 0 & j\frac{1}{2}\omega L_B Y_{12} & -\frac{1}{4}\omega^2 L_C L_B Y_{12} \\ 0 & 0 & Y_{12} & j\omega L_C Y_{12} \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{array}\right.$$

$$\left.\begin{array}{cc|cc} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \hline j\frac{1}{2}\omega L_C Y_{21} & -\frac{1}{4}\omega^2 L_C L_B & 0 & 0 \\ Y_{21} & j\omega\frac{1}{2}L_B Y_{21} & 0 & 0 \\ \hline \left[1+j\frac{1}{2}\omega L_B(Y_{11}+Y_{22})\right] & j\frac{1}{2}\omega L_B\left[2+j\frac{1}{2}\omega L_B(Y_{11}+Y_{22})\right] & j\frac{1}{2}\omega L_B Y_{21} & -\frac{1}{4}\omega^2 L_B L_A Y_{12} \\ (Y_{11}+Y_{22}) & \left[1+j\frac{1}{2}\omega L_B(Y_{11}+Y_{22})\right] & Y_{21} & j\frac{1}{2}\omega L_A Y_{21} \\ \hline j\frac{1}{2}\omega L_A Y_{12} & -\frac{1}{4}\omega^2 L_B L_A Y_{12} & \left(1+j\frac{1}{2}\omega L_A Y_{11}\right) & j\omega L_A\left(2+j\frac{1}{2}\omega L_A Y_{11}\right) \\ Y_{12} & j\frac{1}{2}\omega L_B Y_{12} & Y_{11} & \left(1+j\frac{1}{2}\omega L_A Y_{11}\right) \end{array}\right] \quad (1b)$$

Here Y_{ij} are the Y parameters of the active devices which are assumed to be identical throughout the amplifier.

As mentioned earlier, to extract an expression for the gain from (1) is rather impractical in that it leads to a formula depending on 32 variables. Since, at this point, we are striving for a qualitative solution which helps to explain the principle of operation of our three-tier matrix amplifier, we resort to a highly oversimplified transistor model consisting of only three elements. The model and the circuit when using resistors as terminations of the idle ports are shown in Fig. 3. The transistors are located as indicated in the schematic of Fig. 3(b). Since for reasons of simplicity all capacitances C are chosen to be equal ($C = C_{gs} + C_{ds}$), shunt capacitances, C_{sh}, are required in the gate line of the first tier ($C_{sh1} = C_{ds}$) and in the drain line of the third tier ($C_{sh3} = C_{gs}$). If we further assume that $L_A = L_B = L_C = L$, the number of variables is reduced to 9, namely g_m, L, C, R_D, R_{C0}, R_{Cn}, R_{B0}, R_{Bn}, and R_A. Next, let us examine the amplifier ($n = 3$) shown in Fig. 3(b). With

$$Y_{11} \cong j\omega C_{gs} \tag{2a}$$

$$Y_{12} \cong 0 \tag{2b}$$

$$Y_{21} \cong g_m \tag{2c}$$

$$Y_{22} \cong j\omega C_{ds} \tag{2d}$$

and the insertion of the above-mentioned shunt capacitances C_{sh1} and C_{sh3}, the chain matrix (1b) reduces to

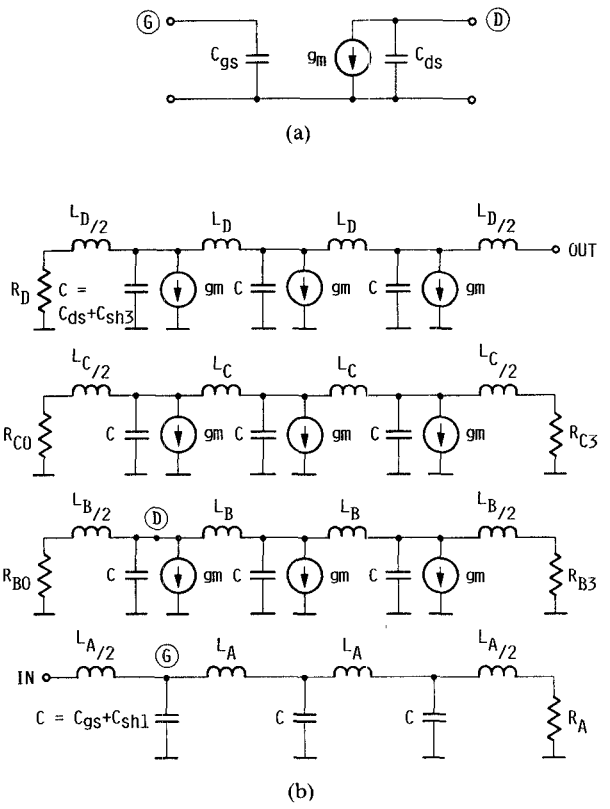


Fig. 3. (a) The idealized MESFET model and (b) the schematic of an elementary version of the matrix amplifier in the form of a 3×3 array.

$$A = \left[\begin{array}{cc|cc|cc|cc}
\left(1-\frac{1}{2}\Omega^2\right) & j\Omega Z_0\left(1-\frac{1}{4}\Omega^2\right) & j\frac{1}{2}\Omega Z_0 g_m & -\frac{1}{4}\Omega^2 Z_0^2 g_m & 0 & 0 & 0 & 0 \\
j\frac{\Omega}{Z_0} & \left(1-\frac{1}{2}\Omega^2\right) & g_m & j\frac{1}{2}\Omega Z_0 g_m & 0 & 0 & 0 & 0 \\
\hline
0 & 0 & \left(1-\frac{1}{2}\Omega^2\right) & j\Omega Z_0\left(1-\frac{1}{4}\Omega^2\right) & j\frac{1}{2}\Omega Z_0 g_m & -\frac{1}{4}\Omega^2 Z_0^2 g_m & 0 & 0 \\
0 & 0 & j\frac{\Omega}{Z_0} & \left(1-\frac{1}{2}\Omega^2\right) & g_m & j\frac{1}{2}\Omega Z_0 g_m & 0 & 0 \\
\hline
0 & 0 & 0 & 0 & \left(1-\frac{1}{2}\Omega^2\right) & j\Omega Z_0\left(1-\frac{1}{4}\Omega^2\right) & j\frac{1}{2}\Omega Z_0 g_m & -\frac{1}{4}\Omega^2 Z_0^2 g_m \\
0 & 0 & 0 & 0 & j\frac{\Omega}{Z_0} & \left(1-\frac{1}{2}\Omega^2\right) & g_m & j\frac{1}{2}\Omega Z_0 g_m \\
\hline
0 & 0 & 0 & 0 & 0 & 0 & \left(1-\frac{1}{2}\Omega^2\right) & j\Omega Z_0\left(1-\frac{1}{4}\Omega^2\right) \\
0 & 0 & 0 & 0 & 0 & 0 & j\frac{\Omega}{Z_0} & \left(1-\frac{1}{2}\Omega^2\right)
\end{array}\right] \tag{3}$$

where

$$\Omega = \sqrt{LC} \tag{3a}$$

and

$$Z_0 = \sqrt{\frac{L}{C}} \tag{3b}$$

are the normalized frequency and the characteristic impedance of the artificial transmission lines.

Using (1a) and (3), it can be shown that there are $2n$ frequencies at which the input and output impedances of an idealized $m \times n$ matrix amplifier based on a simplified network such as that shown in Fig. 3 are purely resistive, regardless of the number of tiers m. They are given in Table I, which presents the roots of the normalized frequencies Ω for the amplifiers with $n = 2$, 3, 4, 5, and 6 elementary cells. Outside of $\Omega = 0$, there is one normalized frequency, namely $\Omega_{n+1} = \sqrt{2}$, that takes a prominent role;

TABLE I
NORMALIZED FREQUENCIES OF THE $m \times n$ MATRIX AMPLIFIER FOR RESISTIVE INPUT AND OUTPUT IMPEDANCES

n \ Ω	= 0	$=\sqrt{2-\sqrt{2+\sqrt{3}}}$	$=\sqrt{2-\sqrt{1/2\,(5+\sqrt{5})}}$	$=\sqrt{2-\sqrt{2+\sqrt{2}}}$	$=\sqrt{2-\sqrt{3}}$	$=\sqrt{2-\sqrt{1/2\,(3+\sqrt{5})}}$	$=\sqrt{2-\sqrt{2}}$	$=\sqrt{2-\sqrt{1/2\,(5-\sqrt{5})}}$	= 1	$=\sqrt{2-\sqrt{2-\sqrt{2}}}$	$=\sqrt{2-\sqrt{1/2\,(3-\sqrt{5})}}$	$=\sqrt{2-\sqrt{3}}$	$=\sqrt{2}$	$=\sqrt{2+\sqrt{2-\sqrt{3}}}$	$=\sqrt{2+\sqrt{1/2\,(3-\sqrt{5})}}$	$=\sqrt{2+\sqrt{2-\sqrt{2}}}$	$=\sqrt{3}$	$=\sqrt{2+\sqrt{1/2\,(5-\sqrt{5})}}$	$=\sqrt{2+\sqrt{2}}$	$=\sqrt{2+\sqrt{1/2\,(3+\sqrt{5})}}$	$=\sqrt{2+\sqrt{3}}$	$=\sqrt{2+\sqrt{2+\sqrt{2}}}$	$=\sqrt{2+\sqrt{1/2\,(5+\sqrt{5})}}$	$=\sqrt{2+\sqrt{2+\sqrt{3}}}$
2	Ω_1	—	—	—	—	—	Ω_2	—	—	—	—	—	Ω_3	—	—	—	—	—	Ω_4	—	—	—	—	—
3	Ω_1	—	—	—	Ω_2	—	—	—	Ω_3	—	—	—	Ω_4	—	—	—	Ω_5	—	—	—	Ω_6	—	—	—
4	Ω_1	—	—	Ω_2	—	—	Ω_3	—	—	Ω_4	—	—	Ω_5	—	—	Ω_6	—	—	Ω_7	—	—	Ω_8	—	—
5	Ω_1	—	Ω_2	—	—	Ω_3	—	Ω_4	—	—	Ω_5	—	Ω_6	—	Ω_7	—	—	Ω_8	—	Ω_9	—	—	Ω_{10}	—
6	Ω_1	Ω_2	—	—	Ω_3	—	Ω_4	—	Ω_5	—	—	Ω_6	Ω_7	Ω_8	—	—	Ω_9	—	Ω_{10}	—	Ω_{11}	—	—	Ω_{12}

it is a solution common to all idealized matrix amplifiers regardless of the number of links and number of tiers. Furthermore, when replacing the idealized device of Fig. 3(a) with a practical MESFET having gate dimensions 0.35 μm $\times$ 200 μm an acceptable gain performance for $n = 3$ can be expected up to $\Omega = \sqrt{2}$. It is for these reasons that we now focus our attention on this frequency ($\Omega = \sqrt{2}$) when deriving a formula for the gain of the idealized 3×3 matrix amplifier of Fig. 3.

Using (1a) and (3) for $n = 3$, we obtain

$$\text{GAIN}(\Omega = \sqrt{2}) \cong |F|^2 (g_m X)^6 \tag{4}$$

where

$$F = F_A [F_{D1}(F_B F_{C1} + F_{C2}) + F_{D2} F_B + F_{D3}] \tag{4a}$$

$$F_A = \frac{2XY_0}{1 + G_A Y_0 X^2} \tag{4b}$$

$$F_{D1} = \frac{(1 - G_D G_{C3} X^2) + j3X(G_{C3} + G_D)}{(1 + Y_0 G_D X^2)} \tag{4c}$$

$$F_{D2} = 4\frac{(1 + G_{B3} G_D X^2)}{(1 + Y_0 G_D X^2)} \tag{4d}$$

$$F_{D3} = -4\frac{(1 - G_A G_D X^2) + jX(G_A + G_D)}{(1 + Y_0 G_D X^2)} \tag{4e}$$

$$F_{C1} = \frac{(1 - G_{B3} G_{C0} X^2) + j3X(G_{B3} + G_{C0})}{(1 + G_{C0} G_{C3} X^2)} \tag{4f}$$

$$F_{C2} = 4\frac{(1 + G_A G_{C0} X^2)}{(1 + G_{C0} G_{C3} X^2)} \tag{4g}$$

$$F_B = \frac{(1 - G_A G_{B0} X^2) + j3X(G_A + G_{B0})}{(1 + G_{B0} G_{B3} X^2)} \tag{4h}$$

$$X(\Omega = \sqrt{2}) = \sqrt{\frac{L}{2C}} \tag{4i}$$

$$Y_0 = 20 \text{ mS}. \tag{4j}$$

As can be seen from (4), even when employing an idealized FET model at a single frequency, the dependency of the linear gain on the terminations and transistor parameters is still rather complicated. Furthermore, an examination of (4) reveals two important corollaries.

1) The linear gain is proportional to $(g_m X)^6$.
2) Short circuits as terminations may be used at one or both terminals of lines B and C. If one terminal of a line is short-circuited, the stability of the amplifier can only be maintained if the other terminal of the same line is terminated into a finite impedance or a short.

While the first result was expected, the second came as a surprise and will be taken advantage of in the amplifier design. The impact on the gain (4) by short-circuiting one of the two idle ports of the lines B and C and varying the termination resistors at the opposite ends is demonstrated in Fig. 4 for the case where the termination resistors R of both lines are identical. Obviously, such a measure will only work at higher frequencies and result in no or little gain at low frequencies, where the gain can be approximated by

$$\text{GAIN}(\Omega = 0) \cong \left[\frac{2(ng_m)^3 Y_0}{(G_A + Y_0)(G_{B0} + G_{Bn} + nG_{ds})(G_{C0} + G_{Cn} + nG_{ds})(G_{D0} + Y_0 + nG_{ds})}\right]^2. \tag{5}$$

Here G_{ds} is the drain–source conductance of the MESFET, and n is the number of MESFET's per tier.

III. CIRCUIT DESIGN

As pointed out in the preceding section, the derived formulas (4) represent qualitative trends rather than an accurate solution. They were developed for the sole pur-

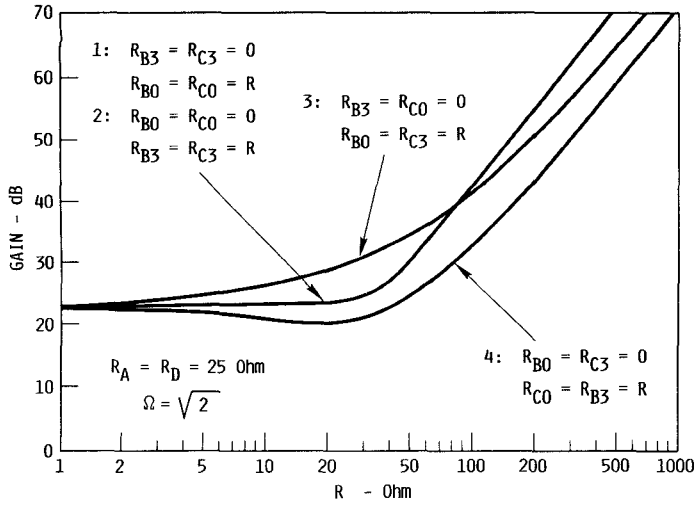


Fig. 4. Gain as a function of the termination resistors R for $R_A = R_D = 25\ \Omega$ at the normalized frequency $\Omega = \sqrt{2}$.

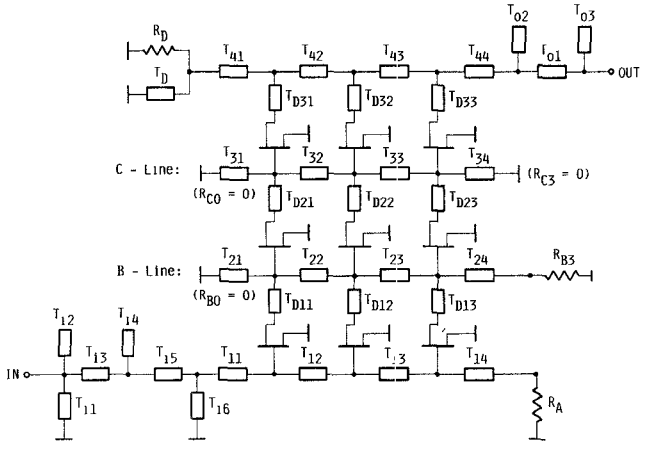
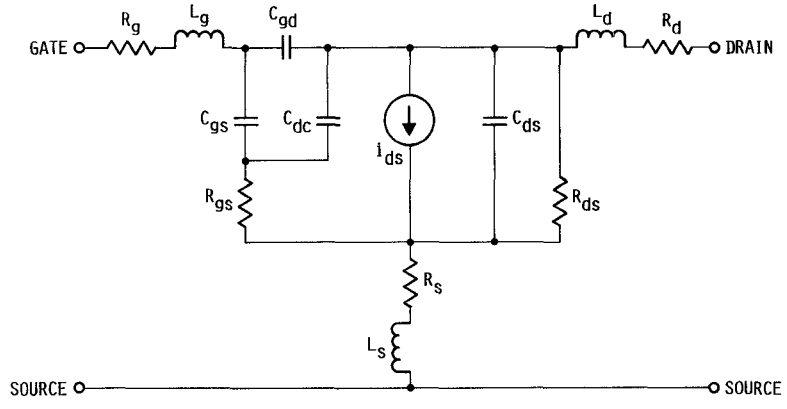


Fig. 5. Schematic of the 3×3 matrix amplifier.



INTRINSIC ELEMENTS			EXTRINSIC ELEMENTS		
gm	=	30.0 mS	R_g	=	6.4 ohm
τ_0	=	1.2 psec	L_g	=	.149 nH
C_{gs}	=	.184 pF	R_s	=	.15 ohm
C_{gd}	=	.013 pF	L_s	=	.032 nH
C_{dc}	=	.047 pF	C_{ds}	=	.010 pF
R_{gs}	=	3.3 ohm	R_d	=	1.5 ohm
R_{ds}	=	290 ohm	L_d	=	.538 nH

Fig. 6. Equivalent circuit and circuit elements of the GaAs MESFET on VPE material.

pose of aiding in the understanding of the amplification mechanism and explaining the rather unorthodox step of using short circuits as the terminations of selected idle ports. With the help of the computer we will now demonstrate that this measure is applicable to all frequencies except for low frequencies ($\Omega < 0.25$), where (5) represents a good approximation for the gain.

The schematic of the 3×3 matrix amplifier chosen for the experimental amplifier is shown in Fig. 5. As can be easily seen, the left port of the B line and both ports of the C line are terminated into short circuits. Instead of lumped elements (inductors), distributed elements (transmission lines) are employed throughout the amplifier. In contrast to the circuit of Fig. 3, this circuit makes use of an input and output matching network in order to improve the reflection coefficients of the amplifier. Biasing of the active devices of the first and second tier is easily accomplished by means of the short-circuited idle ports while the transistors of the third tier are energized through the short-circuit shunt stub parallel to the termination resistor.

In the following, all computations are based on the measured S parameters of the actual MESFET used in our

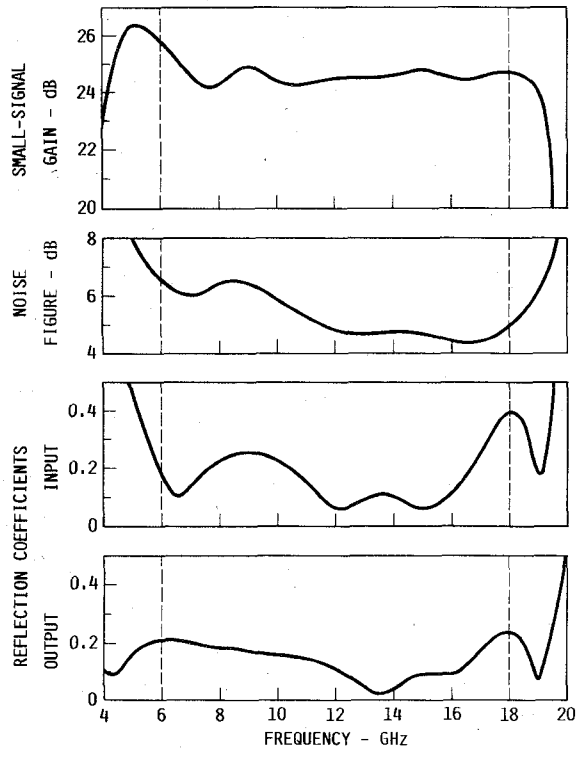


Fig. 7. Optimized performance of the amplifier for $R_{B0} = R_{C0} = R_{C3} = 0$.

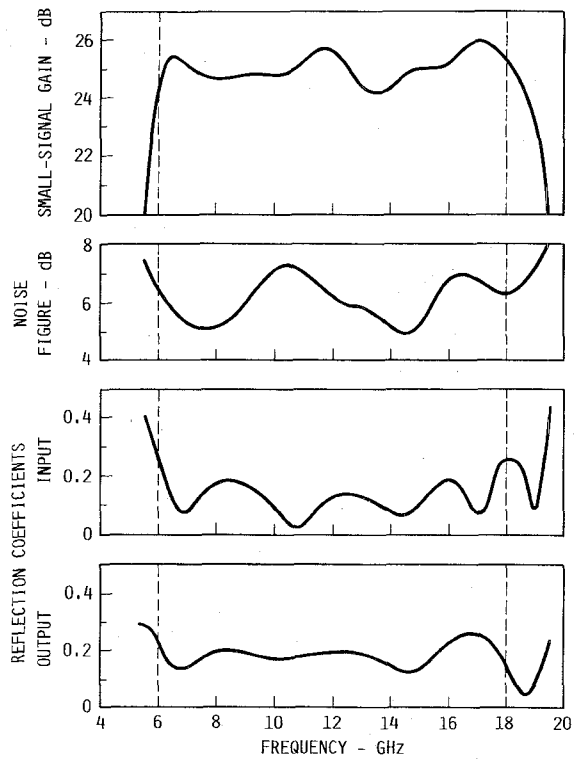


Fig. 8. Optimized performance of the amplifier for $R_{B0} = R_{C3} = 0$.

experiments and were executed using SUPER-COMPACT [5]. The transistor's gate dimensions are 0.35 μm $\times$ 200 μm and its equivalent circuit parameters are represented in Fig. 6. The devices were fabricated on vapor phase expitaxial material. To achieve optimum gain performance, all elements shown in Fig. 5 were subjected to the optimization process for gain and reflection coefficients. Since this process resulted in different transmission line widths and lengths for most linking elements T_{mn}, including T_{21}, T_{31}, and T_{34} (Fig. 5), we may no longer consider T_{21}, T_{31}, and T_{34} simply as links shorted to ground. Observed from a more realistic vantage point, they represent transmission line links terminated by reactances. While terminating all six idle ports of the amplifier with resistors leads to acceptable performance, making use of reactive terminations at selective ports of lines B and C increases the gain at both ends of the frequency band and thereby the unit's bandwidth. The computed performance data of a 3×3 matrix amplifier in accordance with the schematic of Fig. 5, for $R_{B0} = R_{C0} = R_{C3} = 0$, $R_A = 32\ \Omega$, $R_{B3} = 46\ \Omega$, and $R_D = 233\ \Omega$, are plotted in Fig. 7. For comparison, the computed data curves of an amplifier with $R_{B0} = R_{C3} = 0$, $R_{B3} = 53\ \Omega$, $R_{C0} = 57\ \Omega$, $R_A = 29\ \Omega$, and $R_D = 223\ \Omega$ are shown in Fig. 8. The extension of the bandwidth at both ends of the frequency band by choosing $R_{C0} = 0$ in accordance with the circuit of Fig. 5, i.e., $R_{B0} = R_{C0} = R_{C3} = 0$, is clearly discernible when comparing the gain curves of Figs. 7 and 8. For both amplifiers, the results represent a compromise between gain, gain flatness, noise figure, and VSWR. The characteristics exhibited in the data comparison of Fig. 7 and Fig. 8 have been clearly supported by our experiments, as will be demonstrated in the next section.

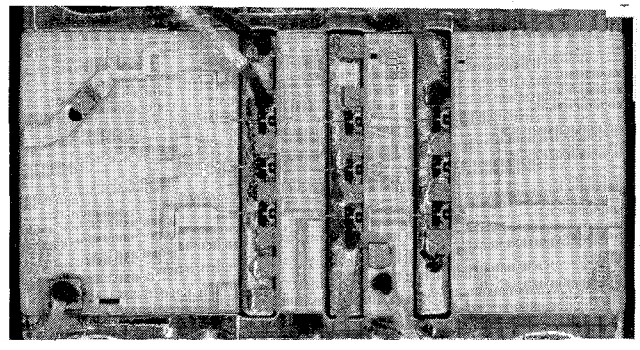


Fig. 9. Photograph of the experimental amplifier.

IV. Experimental Results

A. Data Relevant to the Computed Results of Section III

A photograph of the experimental amplifier designed in accordance with the schematic of Fig. 5 and the computed performance of Fig. 7 is shown in Fig. 9. The circuit is fabricated on four alumina substrates and has the overall dimensions of $0.385 \times 0.175 \times 0.015$ in^3. The unit is self-biased and only one voltage, 13 V, is supplied to this amplifier, which draws a total dc current of 82.5 mA. Approximately 21 percent of the total power consumption is dissipated in the source-bias resistors. The unit's measured termination resistors are $R_A = 29\ \Omega$, $R_{B3} = 49\ \Omega$, and $R_D = 212\ \Omega$ ($R_{B0} = R_{C0} = R_{C3} = 0$) and are within

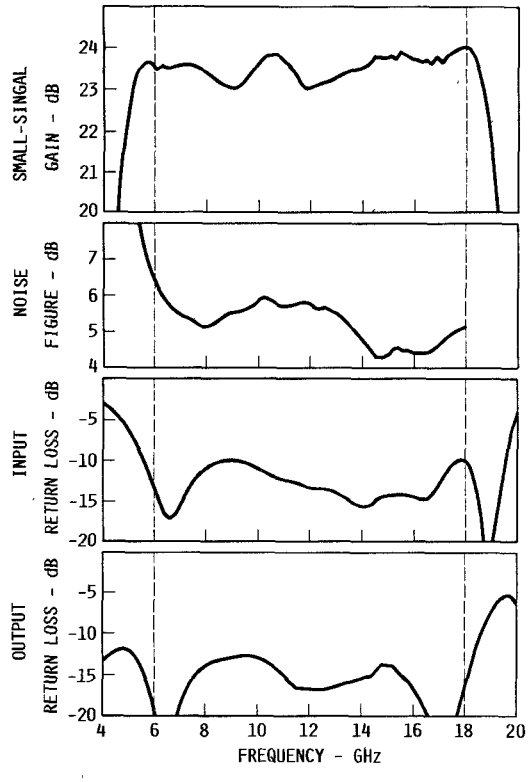


Fig. 10. Measured performance of an experimental amplifier with $R_{B0} = R_{C0} = R_{C3} = 0$ using VPE MESFET's.

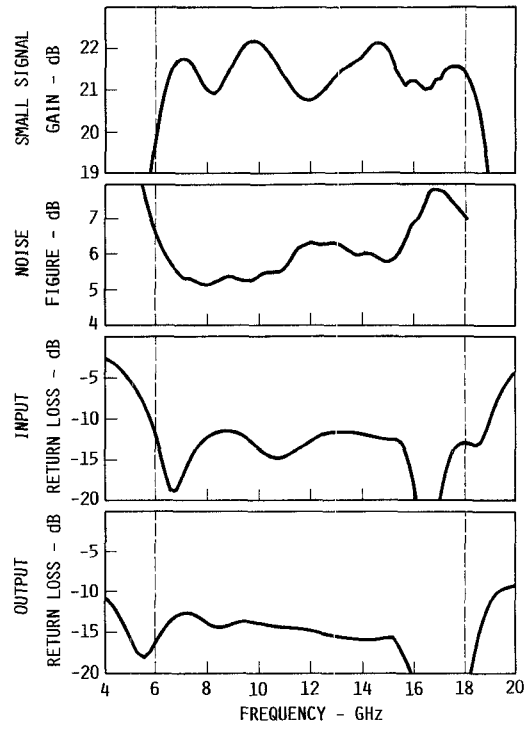


Fig. 11. Measured performance of the experimental amplifier with $R_{B0} = R_{C3} = 0$ using VPE MESFET's.

± 10 percent of the computed values $R_A = 32\ \Omega$, $R_{B3} = 46\ \Omega$, and $R_D = 233\ \Omega$. The measured small-signal gain, noise figure, and return losses are plotted in Fig. 10. A comparison with the computed data of Fig. 7 reveals excellent agreement. For comparison, the curves in Fig. 11 were obtained from an amplifier that has one termination resistor in both lines B and C designed to achieve the performance represented by the computed data of Fig. 8. The termination resistors of the actual amplifier are $R_A = 28\ \Omega$, $R_{B3} = 49\ \Omega$, $R_{C0} = 55\ \Omega$, and $R_D = 207\ \Omega$ ($R_{B0} = R_{C3} = 0$). These values compare to the computed resistances of $R_A = 29\ \Omega$, $R_{B3} = 53\ \Omega$, $R_{C0} = 57\ \Omega$, and $R_D = 223\ \Omega$ discussed in the previous section. As is easily discernible from the plots of Fig. 11 and predicted by the computed results of Fig. 8, the bandwidth is reduced when compared to that of Fig. 10. In addition, the plots of Fig. 11 show a lower gain and a higher noise figure. The measured minimum reverse isolation of both experimental units exceeds -52 dB.

B. Data Obtained Using Improved MESFET's

Subsequent experiments were performed on amplifiers that incorporated MESFET's which were fabricated with the same mask set as the devices employed so far but having MBE rather than VPE material. The resulting transductances g_m and gate–source capacitances C_{gs} were both improved over those of its VPE relative. The outcome of the measurements is believed to be of interest as the MBE devices appreciably improved the amplifier's gain performance, namely, $G = 29.1 \pm 1.1$ dB between 4.6 and 18.3 GHz. The performance of the amplifier is plotted in Fig. 12. This unit's noise figure, however, reached a peak of $NF_{\max} = 7.8$ dB due to the fact that the amplifier was tuned for maximum output power and, like the unit discussed earlier, was not designed for optimum noise performance. A third amplifier tuned for optimum gain and gain flatness exhibited noise figures of $NF = 5.2 \pm 1.2$ dB and gains of 27.7 ± 0.9 dB across the frequency band (Fig. 13).

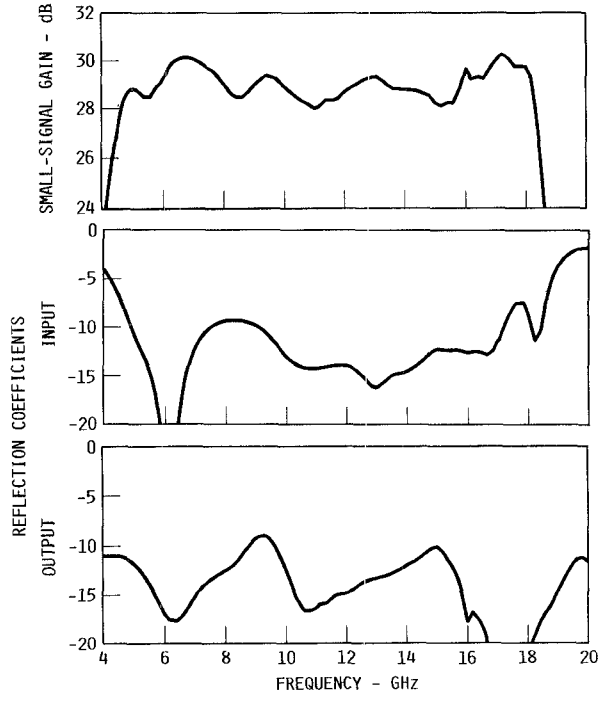


Fig. 12. Measured performance of an experimental amplifier tuned for output power with $R_{B0} = R_{C0} = R_{C3} = 0$ using MBE MESFET's.

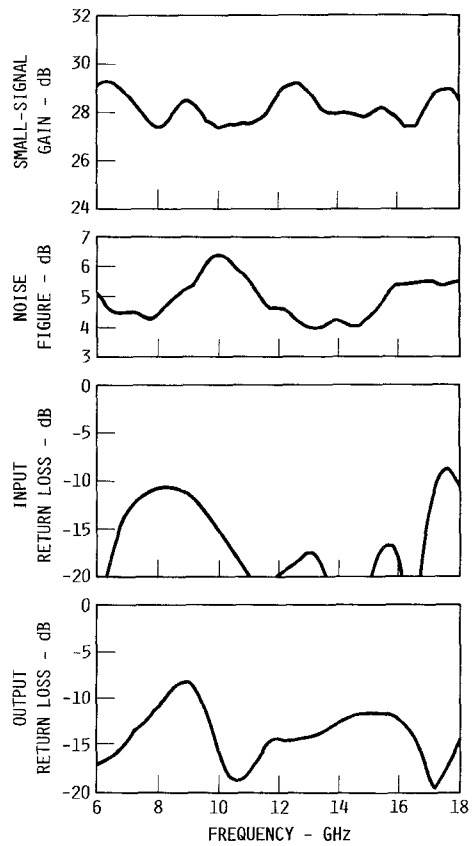


Fig. 13. Measured performance of an experimental amplifier tuned for gain and gain flatness with $R_{B0} = R_{C0} = R_{C3} = 0$ using MBE MESFET's.

C. Comparison of Biasing Schemes

The ensuing power measurements revealed the limitations of the series biasing scheme employed up to this point in time. Some of the experimental results are reflected in the graphs of Fig. 14, in which the output powers and the associated compression levels for series and parallel biasing are compared when operating at a constant input power of $P_{in} = -13$ dBm. Also shown are the relative drain–source voltages V_{DSn}/V_{DSn0}, i.e., the ratios of the drain–source voltages at large-signal and the corresponding drain–source voltages at small-signal operation. The worst-case compression and output power for both biasing schemes occurred at $f = 6$ GHz. At this frequency and for $P_{in} = -13$ dBm, the series biased amplifier was 5 dB into compression at an output power of $P_{out} = 11.5$ dBm. A drive-induced change in the distribution of the dc drain–source voltages is, to a great extent, responsible for the early saturation. The device's drain–source voltage of the third tier was reduced to 57.5 percent of its small-signal level, while that of the second and the first tier increased to compensate for the reduction. The unit's total current shared by all tiers remained between 59.8 mA $\leq I_{BIAS} \leq$ 62.2 mA at small-signal and saturated power levels. The worst-case output power and compression for parallel biasing at $P_{in} = -13$ dBm were 12.8 dBm and 2.8 dB, respectively. Here the dc current of the third tier increased by 19.5 percent from its small-signal level, while that of the

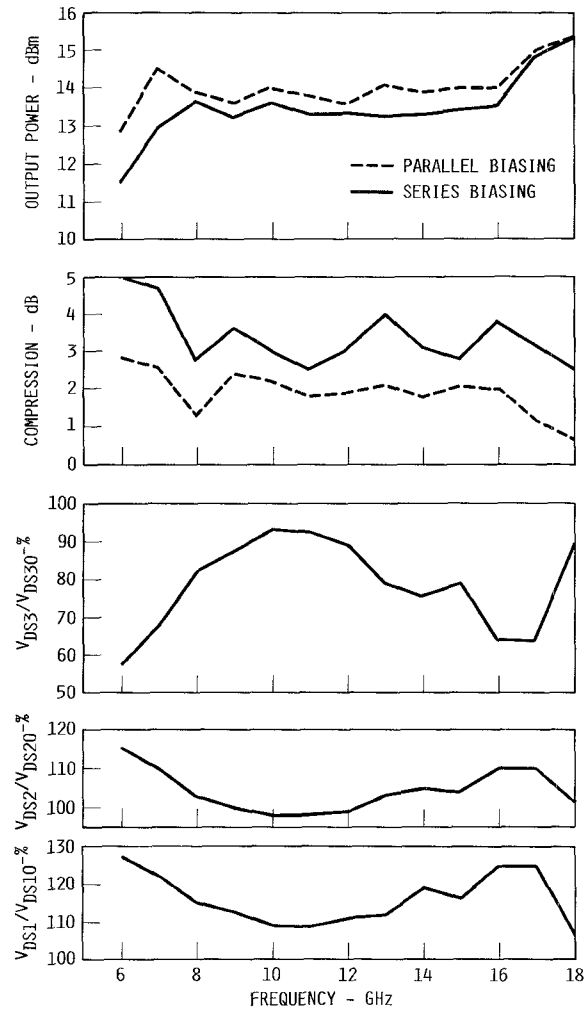


Fig. 14. Compression and output power for series and parallel biasing.

second and the first tier remained virtually unchanged. It becomes evident from these experiments that series biasing of a three-tier matrix amplifier, while capable of operating at low dc currents, results in higher compression and lower output powers when compared with the parallel biased operation. However, in many practical applications, the series biasing is preferred due to its low current requirements.

V. Summary

The main objective of our efforts was to demonstrate the feasibility of the three-tier matrix amplifier as a practical device. This work resulted in the development of two 3×3 amplifiers that yield gains of 23.5 ± 0.5 dB from 5.2 to 18.7 GHz and $G = 29.1 \pm 1.1$ dB from 4.6 to 18.3 GHz, respectively. A third amplifier exhibits a noise figure of $NF = 5.2 \pm 1.2$ dB and a gain of $G = 27.7 \pm 0.9$ dB from 6 to 18 GHz. In order to achieve these performances over the indicated bandwidths, three of the six idle ports of the units were terminated into reactances. An analytical expression of the gain based on an idealized FET model and executed for a particular frequency qualitatively explains the impact of this measure on gain. Subsequent computer

studies demonstrated its feasibility across the frequency band for real devices. Finally, the paper compared the impact of the current-efficient series biasing and the voltage-efficient parallel biasing scheme on the gain compression and the output power of the three-tier matrix amplifier.

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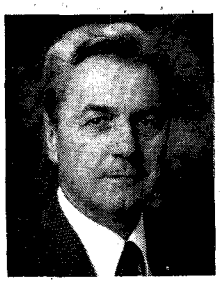
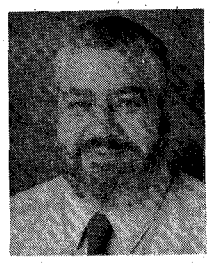


Karl B. Niclas (M'63–SM'80) received the Dipl. Ing. and Doctor of Engineering degrees from the Technical University of Aachen, Aachen, Germany, in 1956 and 1962, respectively.

From 1956 to 1962, he was with the Microwave Tube Laboratory at the Telefunken G.m.b.H. Tube Division, Ulm-Donau, Germany, where he was engaged in research and development on ultra-low-noise and medium-power traveling-wave tubes. In 1958, he became Head of the company's Traveling-Wave Tube Section and Assistant Manager of the Microwave Tube Laboratory. From 1962 to 1963, he was associated as a Senior Project Engineer with the General Electric Microwave Laboratory, Stanford, CA. His work was mainly concerned with theoretical and experimental investigations of single-reversal focused low-noise traveling-wave tube amplifiers and resulted in the first lightweight amplifier of this type. In 1963, he joined the Technical Staff of the Watkins-Johnson Company, Palo Alto, CA, where he is presently Manager, Advanced Development, Devices Group. In this capacity he is responsible for the development of monolithic microwave integrated circuits. His current research efforts are primarily focused on the design of advanced GaAs FET amplifiers in monolithic as well as hybrid technology. From 1967 to 1976, he was Manager of the company's Tube Division. Before that, he was Head of the Low-Noise Tube R&D Section, and prior to that he was engaged in a research program on new concepts for achieving high efficiency in traveling-wave tubes. He is the author of numerous papers in the fields of GaAs FET amplifiers, traveling-wave tubes, and electromagnetic field theory, and he holds a number of patents.

Dr. Niclas was a corecipient of the 1962 Outstanding Publications Award of the German Society of Radio Engineers (NTG) and of the 1985 Microwave Prize awarded by the Microwave Theory and Techniques Society of the IEEE.



Ramon R. Pereira was born in Redwood City, CA, on August 15, 1939.

He has worked at the Watkins-Johnson Company, Palo Alto, CA, since November 1972. Currently assigned to the Devices Group, he has been instrumental in the development of multioctave, cascadable, distributive power, and memory loop amplifiers, as well as other state-of-the-art microwave components. From June 1967 until November 1972, he was with Applied Technology, Inc., Palo Alto, CA, as a Production Leader in charge of oscillator sources and various other solid-state products. Before that, he was engaged in R&D on high-power microwave tubes at Litton Industries, San Carlos, CA.